Longsys Electronics | FORESEE | Longsys Electronics | Longsys江波龙电子

UFS Product Functions

• UFS 2.2 protocol	• Emergency power failure protection	• Supports Write Boost (WB) and Host Performance Boost (HPB)	• FFU upgrade support
• Full-cycle bad block management	• Supports HS-GEAR3	• Supports mainstream compatible platforms	• Supports mainstream compatible platforms
• 2-lane	• LDPC ECC algorithm	• Smart health monitoring	• Global wear balance management

Application Scope

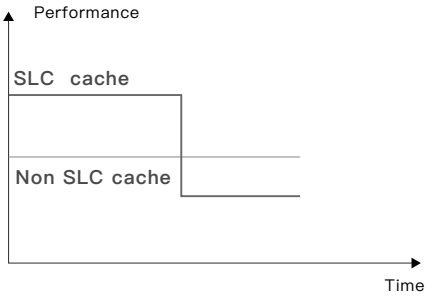
Smartphones | Tablets | High-speed cameras | VRs/ARs | Smart cars

UFS Product Functions

Write Boost(WB)

■ WB uses free block acceleration (FBA) in the FW algorithm and uses multi-level cells (MLCs)/triple-levecells (TLCs) as single level cells (SLCs) to improve read and write performance.

Flash memory type	SLC	MLC	TLC
Number of bits per cell	1	2	3
Read time	25	50	75
Write time	300	600	600
Erase time	1500	3000	4500

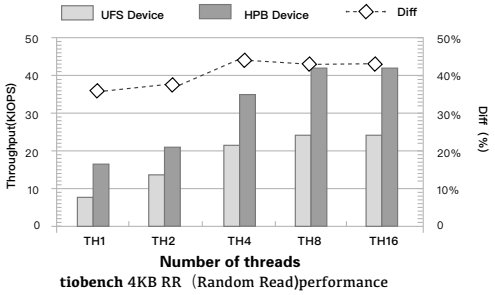


*Note: The above is for reference only. Data may vary according to flash memory.

Host Performance Boost(HPB)

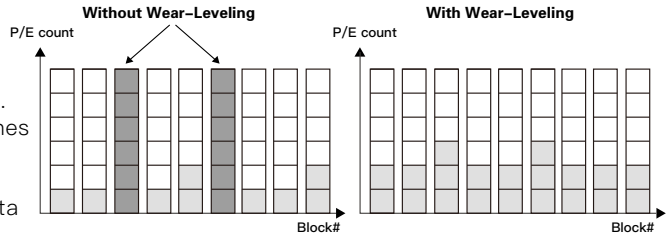
■ Due to fragmentation of mobile phone data storage, the L2P MAP becomes larger with further usage, making it difficult to retrieve data. During random read, the L2P MAP must be loaded frequently, deteriorating read performance.

■ HPB technology reads the L2P MAP to the memory. This allows the host end to have larger memory space and store more L2P MAP data, reducing the UFS burden and improving random read performance.



Wear Leveling

■ When the data write operation is updated continuously, the physical flash memory block is also erased frequently. When the number of times a block has been erased reaches the threshold, the block will be scrapped, reducing the lifespan of flash memory. If all flash memory blocks bear erasing operations together, they can undertake more data write operations.



UFS Line-up

	64GB	128GB	256GB
Part Number	FEUDNN064G-C2A46	FEUDNN128G-C2A44	FEUDNN256G-C2A44
Package	11.5*13*0.8mm	11.5*13*0.8mm	11.5*13*1.0mm
Interface	up to HS-GEAR3 2Lane	up to HS-GEAR3 2Lane	up to HS-GEAR3 2Lane
Nand Flash	3D TLC	3D TLC	3D TLC
Seq. W/R① (2 lane)	Up to 270/960 MB/S	Up to 270/960 MB/S	Up to 500/960 MB/S
Operation Temp(Tc)	-25℃ ~ 85℃	-25℃ ~ 85℃	-25℃ ~ 85℃
Storage Temp(Ta)	-40℃ ~ 85℃	-40℃ ~ 85℃	-40℃ ~ 85℃
Operating voltage	VCC : 2.7 – 3.6V VCCQ2 : 1.7 – 1.95V	VCC : 2.7 – 3.6V VCCQ2 : 1.7 – 1.95V	VCC : 2.7 – 3.6V VCCQ2 : 1.7 – 1.95V
Endurance②	1000 P/E	1000 P/E	1000 P/E
Data Retention	100% P/E:1 years	100% P/E:1 years	100% P/E:1 years

①Test Condition: @25℃,Device level test without file system overhead,Seq.Chunk size 512KB,Cache on. ②WAI=1